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REMARKS

Favorable reconsideration and allowance of claims 13-20 of the present application are respectfully requested.

Claims 13 and 16 have been amended. All claims pending in the present application, i.e. claims 13-20, are now believed to be in condition for allowance.

Claims 13-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Augusto (USP 5,963,800). However, Augusto does not teach each and every element of independent claim 13. For example, Augusto does not teach or suggest the formation of a device having vertical channels. In a vertical channeled device, the direction of current flow is in a horizontal direction. In Augusto, horizontal channeled devices are fabricated. In horizontal channeled devices, the direction of current flow is in a vertical direction. Additionally, Augusto does not teach or suggest a thin vertical channel (FIN) metal oxide semiconductor field effect transistor (MOSFET) which includes, among other differences, insulating spacers that separate a gate region and source/drain diffusion regions, the gate region comprising two regions of gate conductor that are separated from vertical channel regions by an insulating film comprising a gate dielectric. In the claimed structure, the insulating spacers are present in the final FIN MOSFET device shortening the gate length of the MOSFET to sub 0.05 μm.

In accordance with the claimed structure, there is provided a double-gated/double channel FIN MOSFET device in which the gate region is self-aligned to the source/drain

diffusion regions and vertical channel regions.

On the other hand, Augusto provides a SiGe-based vertical metal-insulator-semiconductor field effect transistor (MISFET) device that is short enough to allow ballistic operation, yet attempts to solve the drain induced barrier lowering (DIBL) problem. The term vertical is used in Augusto to describe the direction of current flow. Since a vertical MISFET is disclosed and illustrated, the Augusto device must have a horizontal channel region.

As depicted and described in Augusto, the SiGe-based vertical MISFET devices comprise a stack of several layers which includes at least a source layer, a channel layer and a drain layer confined by a peripheral surface formed by edges of the several layers. The Augusto MISFET devices have a surrounding gate overlapping at least partially the peripheral surface formed by the edges of the several layers of the MISFET device, and a gate insulator positioned between the gate and the peripheral surface. In accordance with Augusto, the process for fabricating such a structure includes the steps of epitaxially depositing the several layers sequentially on a silicon substrate; patterning and etching the several layers to form a plurality of edges, each of the edges defining one part of the peripheral surfaces; forming the insulator on at least a portion of the peripheral surface; and forming the surrounding gate on at least a portion of the insulator.

Applicants observe in a first instance that Augusto does not teach or suggest the presence of vertical channel regions, as presently claimed. In contrast, the channel

regions disclosed in Augusto are horizontal channel regions that are positioned between vertical gate electrodes and insulators. As such, the device being fabricated in Augusto is a different device from that being formed in accordance with claim 13. And since claims 14-20 depend from claim 13, it also differs from the device as claimed in those claims for the same reasons, as well as others.

In view of the above remarks, Applicants submit that the rejection based on Augusto has been overcome.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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